AMENDMENTS TO THE CLAIMS

Please amend the claims as follows.

1. (Currently Amended) A method for optimizing decoupling capacitance in a delay locked loop, comprising:

   inputting a ~~representative~~ digitized power supply waveform having noise to a simulation of the delay locked loop, wherein the digitized power supply waveform is captured prior to starting the simulation;

   estimating jitter of the delay locked loop dependent on the inputting;

   adjusting an amount of decoupling capacitance dependent on the estimating; and

   repeating the inputting, estimating, and adjusting until the jitter falls below a selected amount.

2. (Currently Amended) The method of claim 1, wherein the ~~representative~~ digitized power supply waveform is captured ~~obtained~~ from a physical system.

3. (Original) The method of claim 2, wherein the physical system comprises a printed circuit board.

4. (Original) The method of claim 2, wherein the physical system comprises a chip package.

5. (Original) The method of claim 2, wherein the physical system comprises a chip.

6. (Currently Amended) The method of claim 1, wherein the ~~representative~~ digitized power supply waveform is captured ~~obtained~~ from a location on a physical system adjacent to an intended location of the delay locked loop.

7. (Cancelled)

8. (Cancelled)

9. (Cancelled)

10. (Currently Amended) The method of claim 1, wherein the ~~representative~~ digitized power supply waveform is dependent on at least one selected from the group consisting of temperature, voltage, frequency, and manufacturing process.

11. (Original) The method of claim 1, wherein the simulation of the delay locked loop is dependent on at least one selected from the group consisting of temperature, voltage, frequency, and manufacturing process.

12. (Currently Amended) A computer system for optimizing decoupling capacitance in a delay locked loop, comprising:

a processor;

a memory; and

software instructions stored in the memory adapted to cause the computer system to:

input a ~~representative~~ digitized power supply waveform having noise to a simulation of the delay locked loop, wherein the digitized power supply waveform is captured prior to starting the simulation;

estimate jitter of the delay locked loop dependent on the ~~representative~~ digitized power supply waveform having noise;

adjust an amount of decoupling capacitance dependent on the estimate; and

repeat the input, estimate, and adjust until the jitter falls below a selected amount.

13. (Currently Amended) The computer system of claim 12, wherein the ~~representative~~ digitized power supply waveform is captured from a physical system.

14. (Original) The computer system of claim 13, wherein the physical system comprises a printed circuit board.

15. (Original) The computer system of claim 13, wherein the physical system comprises a chip package.

16. (Original) The computer system of claim 13, wherein the physical system comprises a chip.

17. (Currently Amended) The computer system of claim 12, wherein the ~~representative~~ digitized power supply waveform is captured ~~obtained~~ from a location on a physical system adjacent to an intended location of the delay locked loop.

18. (Cancelled)

19. (Cancelled)

20. (Cancelled)

21. (Cancelled)

22. (Original) The computer system of claim 12, wherein the simulation of the delay locked loop is dependent on at least one selected from the group consisting of temperature, voltage, frequency, and manufacturing process.

23. (Currently Amended) A computer-readable medium having recorded thereon instructions executable by a processor, the instructions adapted to:

input a digitized ~~representative~~ power supply waveform having noise into a simulation of a delay locked loop, wherein the digitized power supply waveform is captured prior to starting the simulation;

estimate jitter of the delay locked loop dependent on the digitized ~~representative~~ power supply waveform having noise;

adjust an amount of decoupling capacitance dependent on the estimate; and

repeat the input, estimate, and adjust until the jitter falls below a selected amount.

24. (Currently Amended) The computer-readable medium of claim 23, wherein the digitized ~~representative~~ power supply waveform is captured ~~determined~~ from a physical system.

25. (Original) The computer-readable medium of claim 24, wherein the physical system comprises a printed circuit board.

26. (Original) The computer-readable medium of claim 24, wherein the physical system comprises a chip package.

27. (Original) The computer-readable medium of claim 24, wherein the physical system comprises a chip.

28. (Currently Amended) The computer-readable medium of claim 23, wherein the digitized ~~representative~~ power supply waveform is captured ~~obtained~~ from a location on a physical system adjacent to an intended location of the delay locked loop.

29. (Cancelled)

30. (Cancelled)

31. (Cancelled)

32. (Currently Amended) The computer-readable medium of claim 23, wherein the digitized ~~representative~~ power supply waveform is dependent on at least one selected from the group consisting of temperature, voltage, frequency, and manufacturing process.

33. (Original) The computer-readable medium of claim 23, wherein the simulation of the delay locked loop is dependent on at least one selected from the group consisting of temperature, voltage, frequency, and manufacturing process.